REMARKS

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang (US 2005/017 5130) in view of Webster, *et al* (hereafter "Webster") (US 2003/007 2284. Applicant submits that as currently amended, claims 1-2, 4, and 6 are not obvious in view of the cited prior art. Applicant traverses the rejection of claims 3 and 5.

With regard to claim 1, Applicant submits that the combination of Yang and Webster fails to teach the required limitations. Furthermore, Applicant submits that there are no teachings in Yang or the art cited by the Examiner that would allow someone of ordinary skill to make the modifications suggested by the Examiner.

First, claim 1 requires a **memory** that stores the polyphase components from at least one polyphase cycle prior to the current polyphase cycle. The Examiner points to Yang (Fig. 2, and page 1 [0008]) identifying buffers 208 and 210 are being equivalent to memory.

Applicant submits that the cited passage makes it clear that the buffers are merely impedance matching devices that operate on differential signals created by the differential mixers from the differential input signal S+ and S-. Moreover, the output of the mixers 204 and 206 are analog signals; hence, the buffers (typical of art prior to the invention of Yang) cannot store the signal. Additionally, Yang teaches away from using the buffers in question, as these buffers use excessive power and cause mismatches between the in-phase and quadrature signals (paragraph [0008]). Furthermore, claim 1 requires a memory that stores **a polyphase component from a previous cycle**. At best, even if the buffers of Yang were to be interpreted as equivalent to a memory, that memory would be storing the output of the mixers from the current cycle, however that cycle is defined.

Hence, Applicant submits that the claim limitation requiring a memory that stores the polyphase components from at least one polyphase cycle prior to the current polyphase cycle is not taught by Yang. Webster does not provide the missing teachings.

Second, claim 1 requires that at each input polyphase cycle, polyphase components are provided by a polyphase component generator. The Examiner points to Yang (Fig. 2, elements and page 1, [0006 – 0007]), identifying mixers 204, 206 as the polyphase component generator.

Applicant submits that in the scheme shown in Figure 2 a differential input signal is downconverted by mixers 204 and 206 which utilize a differential oscillator circuit 202. The Examiner identifies 202 as the clock that defines a sequence of polyphase cycles. However, the Examiner does not point to any teaching of a cycle other than the frequency of the clock. There is no teaching that even one polyphase component is generated **at each cycle** of oscillator 202 by mixers 204, 206. Applicant submits that the polyphase components are generated within PPF 212, according to a clock within that filter. There is no teaching that the clock within the PPF is related to oscillator 202.

Hence, Applicant submits that the claim limitation requiring a polyphase component generator that provides polyphase components at each input polyphase cycle is not taught by Yang. Webster does not provide the missing teachings.

Third, claim 1 requires a plurality of filters, each filter processing a plurality of the polyphase components stored in the memory from a corresponding polyphase cycle. The Examiner points to Yang (Fig. 2, and page 1 [0006], [0008]), identifying PPF 212 as the plurality of filters. Applicant submits that the Examiner has not pointed to any teaching regarding the detailed structure or function of PPF 212 that support the Examiner's identification of this element as the required plurality of filters. Specifically, the Examiner has not pointed to any teaching that 212 even includes a **plurality** of filters, let alone that one of that plurality of filters processes **different** polyphase components **stored in the memory from a single polyphase cycle**.

Hence, Applicant submits that the claim limitation requiring a plurality of filters, each filter processing a plurality of the polyphase components stored in the memory from a

corresponding polyphase cycle is not taught by Yang. Webster does not provide the missing teachings.

Fourth, claim 1 requires a multiplexer that outputs the filtered polyphase components in a predetermined order. The Examiner looks to Webster (Figs. 8a and 13, page 2 [0012], page 7 [0061] and page 9 [0070]) as providing these teachings, identifying switches 809, 1305 as multiplexers, and maintaining that one of ordinary skill would be motivated to modify Yang by adding the multiplexers of Webster. It should be noted that even if one were to accept the Examiner's characterization of Yang, the filtered polyphase components are within PPF 212. Since PPF 212 already outputs a single differential IF signal (IF+, IF- shown in Figure 2) the multiplexer would need to be positioned somewhere within PPF 212. However, Yang does not provide any details of the internal structure of PPF 212, and hence, without further teachings, Applicant submits that one of ordinary skill could not make the modification suggested by the Examiner with any reasonable expectation of success regarding the operability of the resulting system.

Finally, claim 1 has been amended to clarify the nature of the input and output signals. It should be noted that the output signal has been clarified as being an upconverted version of the input signal, and as such, is further differentiated from the teaching of Yang, which teaches a downconverter.

Accordingly, Applicant submits that claim 1 and the claims dependent therefrom are not obvious in view of the cited prior art.

As per claims 3 and 5, the Examiner presents the same arguments for rejection as in the case of claim 1. First, Applicant submits that as the limitations regarding the memory, the polyphase component generator, and the plurality of filters, discussed above with respect to claim 1 are also required in claims 3 and 5, the responses given above with respect to claim 1 are equally relevant in traversing the rejection of claims 3 and 5. Second, regarding the multiplexer requirement, Applicant submits that, as noted above with respect to claim 1, one of ordinary skill

could not make the modification suggested by the Examiner with any reasonable expectation of success regarding the operability of the resulting system.

Third, Applicant submits that these claims require additional limitations, beyond those in common with claim 1, which are not taught by the cited prior art. Claim 3 requires that the memory comprises a shift register, while claim 5 requires the generation of a filtered polyphase component that depends on a non-linear combination of the polyphase components. First, the Examiner has not pointed to any teaching that the buffer (Yang Figure 2, 208, 210) identified by the Examiner as the required memory comprises a shift register. Furthermore, since the buffers are analog devices, it is no clear how one would modify these buffers so as to include a shift register.

With respect to Claim 5, the Examiner has not pointed to any teaching in either reference with respect to generating a filtered polyphase component that depends on a non-linear combination of the polyphase components. It should be noted that Webster teaches filters that utilize a linear combination of the polyphase components. Accordingly, Applicant submits that the Examiner has not made a *prima facie* case for obviousness with respect to claims 3 and 5.

With respect to Claim 2, the Examiner maintains that Yang teaches each filter utilizes the same functional relationship to generate the filtered polyphase components. The Examiner points to page 8, [0062] as supporting this assertion. First, there is no page 8 or paragraph [0062] in Yang. Applicant assumes that the Examiner meant to refer page 8, parapgraph [0062] of Webster. Figure 8B shows a conventional finite impulse filter that forms a linear filtered component using a linear combination of the polyphase components to shape a pulse. It should be noted that the coefficients $C_{i,j}$ shown in Figure 8 are different for each polyphase filter. The Examiner has not pointed to any teaching in Webster that $C_{i,j}$ is equal to $C_{k,j}$ for i different from k. Hence, the filters do not use the same functional relationships. Hence, there are additional grounds for allowing Claim 2.

With respect to Claim 4, the Examiner points to Webster as teaching a finite impulse response filter. The issue is not whether a finite impulse filter that operates on polyphase components is known. The issue is whether one would modify PPF 212 shown in Yang to utilize a plurality of such filters. The Examiner has not pointed to any teaching that such a filter network could be utilized with the differential signals taught in Yang to provide the differential IF signal in Yang. Hence, there are additional grounds for allowing Claim 4.

With respect to Claim 6, the Examiner states that Yang teaches that the polyphase component generator identified by the Examiner receives one pair of digital signal in each polyphase cycle. The "polyphase component generator" identified by the Examiner is a pair of analog mixing circuits operating on a differential signal to generate two downcoverted analog differential signals. The input is a single analog differential signal S+, S-. Hence, there are additional grounds for allowing Claim 6.

Respectfully Submitted,

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